

U.S. Department of Commerce, Patent and Trademark Office				Attorney Docket No.: 026-0002-1		
				Application No.: Not Yet Assigned		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s): Michael Perrott et al.		
(Use several sheets if necessary)				Filing Date: Herewith		
				Group Art Unit: Not Yet Assigned		
				Date Submitted: September 5, 2003		
U.S. Patent Documents						
*Examiner Initial	AA	Document Number	Date	Name		
RM	AA	6,150,891	Nov. 21, 2000	Welland et al.		
RM	AB	6,167,245	Dec. 26, 2000	Welland et al.		
LM	AC	6,147,567	Nov. 14, 2000	Welland et al.		
LM	AD	6,137,372	Oct. 24, 2000	Welland et al.		
LM	AE	6,075,416	Jun. 13, 2000	Dalmia		
LM	AF	6,075,388	Jun. 13, 2000	Dalmia		
LM	AG	6,008,703	Dec. 28, 1999	Perrott et al.		
LM	AH	5,027,085	Jun. 25, 1991	DeVito		
LM	AI	5,036,298	Jul. 30, 1991	Bulzachelli		
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		Document	Date	Country	Yes	No
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LM	AR	Andersson, L. I. et al, "Silicon Bipolar Chipset for SONET/SDH 10 Gb/s Fiber-Optic Communication Links," IEEE Journal of Solid-State Circuits, Vol. 30, No. 3, Mar. 1995, pp. 210-218.				
LM	AS	Belot, D. et al., "A 3.3-V Power Adaptive 1244/622/155 Mbit/s Transceiver for ATM, SONET/SDH," IEEE Journal of Solid-State Circuits, Vol. 33, No. 7, Jul. 1998, pp. 1047-1058.				
LM	AT	Gray, C. T. et al., "A Sampling Technique and Its CMOS Implementation with 1 Gb/s Bandwidth and 25 ps Resolution," IEEE Journal of Solid-State Circuits, Vol. 29, No. 3, Mar. 1994, pp. 340-349.				
Examiner		Date Considered				
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NON PATENT LITERATURE DOCUMENTS		
*Examiner Initial	Cite No.	(Including name of author in capital letters, title of article, title of item, date, pertinent pages, volume-issue number(s), publisher, city and/or country where published.)
RM	AA	Gutierrez G. et al, "2.488 Gb/s Silicon Bipolar Clock and Data Recovery IC for SONET (OC-48)," IEEE 1998 Custom Integrated Circuits Conference, pp. 575-578.
LM	AB	Gutierrez, G. and Kong, S., "Unaided 2.5 Gb/s Silicon Bipolar Clock and Data Recovery IC," VIII-7, 1998 IEEE Radio Frequency Integrated Circuits Symposium, pp. 173-176.
LM	AC	Hogge, Charles R., Jr., "A Self Correcting Clock Recovery Circuit," IEEE Journal of Lightwave Technology, Vol. LT-3, Dec. 1985, pp. 1312-1314, re-printed as pp. 249-251.
LM	AD	Hu, T. H. and Gray, P. R., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2- μ m CMOS," IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, Dec. 1993, pp. 1314-1320.
LM	AE	Jarman, David, "A Brief Introduction to Sigma Delta Conversion," Application Note AN9504, Intersil Corporation, May 1995, pp. 1-7.
LM	AF	Kawai, K. et al., "A 557-mW, 2.5-Gbit/s SONET/SDH Regenerator-Section Terminating LSI Chip Using Low-Power Bipolar-LSI Design," IEEE Journal of Solid-State Circuits, Vol. 34, No. 1, Jan. 1999, pp. 12-17.
LM	AG	Lee, T. H. and Bulzacchelli, J. F., "A 155-MHz Clock Recovery Delay- and Phase-Locked Loop," IEEE Journal of Solid-State Circuits, Vol. SC-27, Dec. 1992, pp. 1736-1746, re-printed as pp. 421-430.
LM	AH	Lee, T. H. et al., "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM," IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, Dec. 1994, pp. 1491-1496.
LM	AI	Perrott, M. et al., "A 27mW CMOS Fractional-N Synthesizer/Modulator IC," 1997 IEEE International Solid-State Circuits Conference, Session 22, Communications Building Blocks II, Paper SP 22.2, 1997 Digest of Technical Papers, Vol. 40, pp. 366-367, 487.
LM	AJ	Perrott, M. et al., "A 27mW CMOS Fractional-N Synthesizer Using Digital Compensation for 2.5-Mb/s GFSK Modulation," IEEE Journal of Solid-State Circuits, Vol. 32, No. 12, Dec. 1997, pp. 2048-2060.
LM	AK	Pottbacker, A. et al., "A Si Bipolar Phase and Frequency Detector IC for Clock Extraction up to 8 Gb/s," IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, Dec. 1992, pp. 1747-1751.
LM	AL	Razavi, Behzad, "Design of Monolithic Phase-Locked Loops and Clock Recovery Circuits--A Tutorial," Monolithic Phase-Locked Loops and Clock Recovery Circuits--Theory and Design, ed. B. Razavi, IEEE Press, N.Y., 1996, pp. 1-39.
LM	AM	Walker, R. C. et al., "A 10Gb/s Si-Bipolar TX/RX Chipset for Computer Data Transmission," IEEE International Solid-State Circuits Conference, Session 19, Paper 19.1 Slide Supplement, 1998, pp. 19.1-1 - 19.1-11.
LM	AN	Walker, R. C. et al., "A 1.5 Gb/s Link Interface Chipset for Computer Data Transmission," IEEE Journal on Selected Areas in Communications, Vol. 9, No. 5, June 1991, pp. 698-703.
LM	AO	Weston, H. T. et al., "A Submicrometer NMOS Multiplexer-Demultiplexer Chip Set for 622.08-Mb/s SONET Applications," IEEE Journal of Solid-State Circuits, Vol. 27, No. 7 Jul. 1992, pp. 1041-1049.
LM	AP	Willingham, S. et al., "An Integrated 2.5GHz $\Sigma\Delta$ Frequency Synthesizer with 5 μ s Settling and 2Mb/s Closed Loop Modulation," 2000 IEEE International Solid-State Circuits Conference, Session 12, Paper TP 12.3, pp. 200-201, 457.
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LM	AC	5,559,841	Sep 24, 1996	Pandula		
LM	AD	6,125,158	Sep. 26, 2000	Carson et al.		
LM	AE	6,151,152	Nov. 21, 2000	Neary		
LM	AF	6,208,211 B1	Mar. 27, 2001	Zipper et al.		
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LM	AS	Shayan, Y. R. et al., "All Digital Phase-Locked Loop: Concepts, Design and Applications," IEEE Proceedings-F/Radar and Signal Processing 136, Stevenage, Herts, GB, vol. 136, no. 1, Part F, 1 Feb. 1989, pp. 53-56.				
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